Design Document

**Forward Error Correction and Interleaving in**

**Amateur Radio Satellite Telemetry**

Submitted To:

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Senior Design Project I and II

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**Executive Summary**

Table of Contents

[1. Problem 5](#_Toc371847903)

[1.1. Overall Objectives 5](#_Toc371847904)

[1.2. Historical and Economic Perspective 5](#_Toc371847905)

[1.3. Candidate Solutions 6](#_Toc371847906)

[1.3.1. BPSK modulator 6](#_Toc371847907)

[1.3.2. BPSK demodulator 7](#_Toc371847908)

[1.3.3. Carrier Recovery using Squaring Loop 7](#_Toc371847909)

[1.3.4. Carrier Recovery using Costas Loop 8](#_Toc371847910)

[1.3.5. Timing Recovery 9](#_Toc371847911)

[1.3.6. BFSK Modulation 9](#_Toc371847912)

[1.3.7. BFSK Demodulation 10](#_Toc371847913)

[1.4. Proposed Solution Concept 11](#_Toc371847914)

[1.5. Major Design and Implementation Challenges 12](#_Toc371847915)

[1.6. Implications of Project Success 12](#_Toc371847916)

[2. DESIGN REQUIREMENTS 12](#_Toc371847917)

[2.1. Functional Design Constraints 12](#_Toc371847918)

[2.2. Non-Functional Design Constraints 12](#_Toc371847919)

[3. APPROACH 13](#_Toc371847920)

[3.1. Software Simulation Using Matlab/Simulink 13](#_Toc371847921)

[3.1.1. FSK Modem 13](#_Toc371847922)

[3.1.2. BPSK Modem 13](#_Toc371847923)

[3.1.3. Interleaving FEC 13](#_Toc371847924)

[3.2. Hardware Implementation using ISE Design Suite 13](#_Toc371847925)

[4. EVALUATION 13](#_Toc371847926)

[5. SUMMARY AND FUTURE WORK 13](#_Toc371847927)

[6. ACKNOWLEDGEMENTS 13](#_Toc371847928)

[7. REFERENCES 14](#_Toc371847929)

# Problem

## Overall Objectives

It has been shown that forward error correction dramatically improves bit error rate performance (BER) in amateur packet radio satellite telemetry links (Hsiao, et. al, 2000). Additionally, it has been shown that binary phase shift-keying (BPSK) modulation is more reliable and bandwidth-efficient than audio frequency shift keying (AFSK) modulation (Hsiao, et. al, 2000). Being that average amateur satellite telemetry benefits from neither of these facts, this senior design project aims to demonstrate the degree to which forward error correction and interleaving techniques with BPSK modulation can improve the reliability of the average amateur satellite telemetry link. Consequently, this senior design project advocates for improved robustness in amateur packet radio communication systems, specifically in those systems dealing with satellite telemetry.

Amateur packet radio satellite telemetry is often unidirectional (simplex) and does not benefit from automatic repeat request (ARQ) like in other bidirectional (duplex) amateur packet radio communications (Hsiao, et. al, 2000). In other words, if even one bit of an AX.25 telemetry packet is received in error, the entire packet is discarded and cannot be re-transmitted (Karn, 1994). This means that beacon signals from the amateur satellites must be transmitted with enough power to ensure that the embedded telemetry packet is received without error (de Milliano, et. al, 2010). BPSK modulation with forward error correction combined with interleaving can supersede AFSK, resulting in greatly improved network reliability and power-efficiency in amateur packet radio satellite telemetry. The enhanced network reliability could lower overall power consumption in amateur telemetry satellites (de Milliano, et. al, 2010), resulting in two benefits: 1) reduced cost of satellite construction, and 2) making amateur telemetry satellites more technologically and financially accessible to amateur satellite operators by reducing the size, cost, and complexity of ground station antennas (Karn, 2011).

Hence, the ultimate goal of this senior design project is to demonstrate the improved network reliability and power-efficiency that results from implementing forward error correction and interleaving with BPSK modulation in amateur packet radio telemetry satellites and ground stations.

## Historical and Economic Perspective

The standard digital modulation scheme used for amateur radio very-high frequency (VHF) and ultra-high frequency (UHF) operation is Bell 202 (Capitaine, et. al, 2010). Bell 202 is AFSK modulation using 1200 Hz and 2200 Hz tones, with a resulting data rate of 1200 bit/s. It is typically used in the physical layer of the AX.25 data link layer protocol and this has been the case since the early 1980s (Karn, 1994). In 1984, when Bell 202 was a fairly new standard in the amateur radio community, Steve Goode, K9NG, performed an exhaustive bit error rate (BER) performance analysis of a standard Bell 202 modem (Goode, 1984). Goode found that at least 25 dB of FM receiver quieting (25 dBQ) was necessary for high communication reliability. In other words, 25 dBQ or greater was required to accurately receive 98% of incoming packets, which corresponded to a BER of 1.6e-5. Ralph Wallio, WORPK, figured out that with this BER, there is only a 1.603% chance of accurately receiving 117 consecutive 256-byte AX.25 packets (Wallio). Wallio concluded that “this is as Goode as it gets” and it is virtually impossible to get better results without error correction.

This poor reliability performance is not exclusive to amateur radio terrestrial communications. In 1995, it was demonstrated that error detection alone is not robust enough for amateur radio microsatellite communications also (Hsiao, et. al, 2000). Particularly in simplex satellite communications, the harsh environmental conditions and the microsatellite’s characteristically low transmitter power make for very unreliable telemetry data links (Hsiao, et. al, 2000). It has been demonstrated that forward error correction, specifically convolutional encoding and decoding, can generally correct up to 75 percent of errors (Hsiao, et. al, 2000). It was also demonstrated that 1200 bit/s BPSK provides much more reliable transmission quality than 1200 bit/s AFSK, irrespective to whether the VHF or UHF amateur bands are used. Moreover, it was demonstrated that BPSK occupies a considerably smaller frequency bandwidth than AFSK while possessing excellent anti-interference properties. And with a general tenfold BER performance increase for both 1200 bit/s AFSK and BPSK over 144 MHz VHF, implementing forward correction for amateur satellite telemetry was clearly demonstrated to be better than not implementing forward error correction.

In 2003, the AAU-Cubesat was one of the first pico-satellites to be launched into space. Moreover, the miniaturized satellite harbored a communication subsystem that implemented both forward error correction and interleaving over 9600 bit/s Gaussian minimum shift-keying (GMSK) AX.25 (Alminde, et. al, 2002). The enhanced robustness and data rate was justified by the fact that it had to transmit approximately 1461 kilobytes (kB) of telemetry and picture data per day. This simply would not have been possible had the satellite not utilized error detection and correction. However, it operated at 437.9 MHz, meaning that it was particularly difficult for the average amateur radio operator with a 2-meter radio transceiver to receive its telemetry data. This would particularly bother Phil Karn, KA9Q, who is a strong proponent of making robust satellite telemetry links accessible to the average amateur radio operator (Karn, 2011). Karn asserts that robust telemetry links (using forward error correction) reduce the cost of satellite construction and simplify ground antennas, making amateur radio satellite telemetry much more technologically and financially accessible to amateur satellite operators (Karn, 2011).

As amateur satellite designers foresee the next generation of miniature satellites (de Milliano, et. al, 2010), and as the next generation of amateur satellites equipped with robust communication schemes continue to ascend into space, and as miniature satellites become increasingly more financially and technologically accessible to amateur satellite operators, it must be clearly demonstrated to the amateur radio community how these advancements trump the ubiquitous 1200 bit/s AFSK AX.25. Hence, to reiterate, this senior design project hopes to clearly demonstrate the performance advantages that yield from using forward error correction and interleaving schemes with BPSK modulation in amateur satellite telemetry.

## Candidate Solutions

This senior design project will determine the telemetry packet error rate (PER) performance and the coding gain due to implementing forward error correction in amateur radio satellite telemetry. These two parameters, respectively, will allow us to compare the reliability and power-efficiency between using and not using FEC in amateur radio satellite telemetry. This implies that we will be comparing several digital communication systems. In this senior design project, three digital communication systems will be developed for modeling amateur radio satellite telemetry. The first system (System A) will replicate most amateur radio satellite telemetry links that exist today – 1200 bit/s Bell 202 modulation without FEC. The second system (System B) exploit the fact that BPSK modulation is better than AFSK in amateur VHF and UHF operations (Hsiao, et. al, 2000) – 1200 bit/s BPSK without FEC. The third system (System C) will be a robust version of the second system – 1200 bit/s BPSK with FEC.

Each of the three digital communication systems will represent simplex amateur satellite telemetry over a transmission medium (i.e., AWGN). We have chosen to use the AWGN channel model to represent our transmission medium because , compared to other channel models, it provides maximum bit corruption and it is assumed that systems that perform well in AWGN perform well in real-world scenarios (Viswanathan, 2013). Additionally, AWGN is a good model for many satellite communication links including amateur radio satellite telemetry (Viswanathan, 2013). Hence, no other satellite telemetry phenomena, such as interference, distortion, fading, or Doppler shift, will be modeled in this senior design project. Each system will form a digital loopback for BER performance analysis. Each system will contain a modulator (at the transmitter), a demodulator (at the receiver), a simulated transmission medium (i.e., AWGN), and a bit error rate tester (BERT) in software via PC. Additionally, the third system (System C) will also implement forward error correction. The three systems are outlined below:

1. **System A**
   1. Transmitter
      1. AX.25 packet generator (BERT)
      2. Bell 202 modulator (1200 bit/s)
   2. AWGN Channel
   3. Receiver
      1. Bell 202 AFSK demodulator (1200 bit/s)
      2. AX.25 packet comparator (BERT)
2. **System B**
   1. Transmitter
      1. AX.25 packet generator (BERT)
      2. BPSK modulator (1200 bit/s)
   2. AWGN Channel
   3. Receiver
      1. BPSK demodulator (1200 bit/s)
      2. AX.25 frame comparator (BERT)
3. **System C**
   1. Transmitter
      1. AX.25 packet generator (BERT)
      2. FEC engine (send)
      3. BPSK modulator (1200 bit/s)
   2. AWGN Channel
   3. Receiver
      1. BPSK demodulator (1200 bit/s)
      2. FEC engine (receive)
      3. AX.25 packet comparator (BERT)

### System A (BPSK modulator)

The design of any modem requires two fundamental components, a modulator and demodulator. The modulator is responsible for taking baseband data and either source encoding it, or translating it to passband levels necessary for radio transmission. In the history of digital communication, there are many line codes that have been developed. Each of them has their own benefits as far as bandwidth requirements or self-clocking characteristics. Listed below are just a few of the more common line codes typically encountered in a communication systems:

1. Return to Zero (RZ)
2. Non-Return to Zero (NRZ)
3. Non-Return to Zero-Inverted (NRZI)
4. Bi-phase Manchester

Our modem was designed to interface between the TNC and the transceiver. This means our modem will only perform baseband modulation. From the TNC, the modem receives AX.25 data streams and further processes them using a bi-phase Manchester encoder. The benefit of bi-phase Manchester code is that it is self-clocking which makes timing synchronization easier on the receiving end.

### System A (BPSK demodulator)

The demodulator is responsible for providing either coherent or non-coherent demodulation. Coherent demodulators require phase synchronization between the received signal and the locally generated oscillator. Conversely, Non-coherent demodulation does not require synchronization and makes no attempt to estimate the phase of the received signal. The advantage of non-coherent modulation is that it does not require additional hardware like phase-locked loops which are used to lock onto the incoming carrier phase. However, the LEO-AMSAT’s we are interested in communicating with use BPSK for downlink and thus requires the design of a coherent demodulator.

The successful extraction of information from a received signal in a coherent demodulator requires both carrier and timing synchronization. Figure 1 illustrates the architecture of a typical coherent demodulator.



Figure 1. Received waveform takes two paths. First path extracts carrier for coherent demodulation and the second path recovers timing information. This architecture is based on the optimum binary receiver

The received signal from the transceiver is first processed by a band pass filter to remove as much noise as possible and then sent to the carrier recovery circuit. Recovering the carrier is done in one of two ways, the squaring loop or the Costas loop. Each method utilizes phase-lock concepts and has its own advantages and disadvantages in terms of complexity and performance.

**Carrier Recovery using Squaring Loop**

The squaring loop is a popular choice for coherent demodulation of BPSK waveforms. It’s mathematically easy to analyze and its hardware implementation is not as complex as the Costas loop. As the name implies, the received signal is squared to remove any phase offsets and then processed by a bandpass filter to remove as much noise as possible. After the band pass filter, the signal is fed to a phase-lock loop (PLL) for phase and frequency tracking. Once the output of the voltage controlled oscillator (VCO) is locked in phase and frequency with the received signal, its frequency is divided by two. The resulting carrier is fed back to the mixer where it is mixed with the received waveform and the timing can be recovered. The operation of the squaring is shown in Figure 2.



Figure 2. Squaring loop used for carrier recovery in the coherent demodulator. The Phase-Lock Loop utilizes feedback to track and lock onto in the received waveforms suppressed carrier

**Carrier Recovery using Costas Loop**

Another method for carrier recovery was proposed by John P. Costas in his 1957 paper, *Synchronous Communication*. Unlike the squaring loop whose only purpose is suppressed carrier reconstruction, the Costas loop is capable of synchronous data detection in addition to suppressed carrier reconstruction. One of its disadvantages is its mathematical complexity compared to the squaring loop, but in terms of hardware components needed for complete coherent demodulation, they both require approximately the same amount.



Figure 3. Costas loop used for suppressed carrier reconstruction as well as synchronous data detection.

Coherent modulation utilizing the Costas loop would require one band-pass filter, three low-pass filters, three multipliers and a VCO. Likewise, the squaring loop would also require one band-pass filter, three multipliers (including the squarer) and a VCO. Instead of three low-pass filters needed by the Costas, the squaring loop only requires two. Note also that the squaring loop requires a flip-flop for frequency division, but with today’s FPGA’s, a single flip-flop is negligible. The decision for implementing the squaring loop versus the Costas loop will ultimately be decided by their tracking and locking performance in the presence of noise and Doppler shifts (See section 1.5, Major Design and Implementation Challenges).

**BPSK demodulator - Timing Recovery**

### Systems B & C (BFSK Modulation)

The BFSK modem abides by the Bell 202 standard which uses frequencies of 1200 Hz for Mark (*b0*) and 2200 Hz for Space (*b1*). Following this protocol, the phase of the signal can be implemented either coherently or non-coherently. A coherent modulation (continuous phase modulation) implies that the phases of the two signals are always equal, which inherently prevents discontinuous jumps between a Mark and Space. Conversely, non-coherent FSK modulates the two signal waveforms without any effort to match the two signals’ phase, hence the modulated signal may experience discontinuous jumps in phase.

Coherent FSK modulators tend to consist of several complicated components, are not commonly used to avoid unnecessary loss of power although they yield a better BER performance (Rao, 1990). Non-coherent FSK modulation is simpler to implement and is commonly used in several modulation. However, with the technological development, coherent modulation can surely be implemented with as much efficiency as the non-coherent modulation.

**Non-coherent modulation**

As previously mentioned, coherent modulation requires continuous phase of the modulated signal, which can involve complicated hardware or algorithms. As a result, it is common to ignore the phase of the signals and directly modulate the two signals. This implies that the phase modulated signal will be subject of random variations. The non-coherent modulator can be implemented using the two sinusoidal wave generators (sine functions) and a multiplexer controlled by the input data *m(t)*. Switching between the frequencies will generate a BFSK waveform with a bit period equal to the periodicity of the switches.



Figure 4. BFSK modulator used in non-coherent modulators. The data *m(t)* controls the output of the multiplexer at data’s baud rate.

**VCO Coherent modulation**

Non-coherent waveforms originate from the fact that two signal sources are used to modulate the data, therefore the phase resulting from the modulator varies with the phases of the two tones. Therefore, we expect that continuous phase can be obtained when using a single sinusoidal generator to modulate with two different frequencies. Voltage Control Oscillators

### Systems B & C (BFSK Demodulation)

In the case of the coherent modulator, implementing a continuous phase BFSK waveform may involve complicated elements to track the phase; however, a continuous phase waveform or (glitch free) will enhance error performance compared to the non-coherent modulator. It is very common to implement the coherent modulator using a Voltage Controlled Oscillator (VCO) to output the sinusoidal corresponding to the Mark and Space. Since the VCO is dictated by Eq. only one sinusoidal wave generator is necessary to create two signals.

The Bell 202 Protocol is quite inefficient due to the frequency deviation and the ratio between the data rate and carrier frequency. The Bell 202 modem uses frequencies with a small frequency deviation from the carrier frequency. with very smal the Bell 202 modem The frequencies selected to represented two symbols result in a signal space that is difficult to optimize since the frequencies are not orthogonal. The minimum frequency separation is denoted in equations (1) and (2) below (Nguyen, 2009).



Figure 5. Coherent modulator for BFSK. The data *m(t)* controls the output of the VCO through Eq.

**Non-Coherent Demodulation**

Similar to the modulator, the demodulator can be classed into a coherent modulator and a non-coherent demodulator. In the coherent demodulator, the phases of the modulated signal is either known or is extracted prior to demodulation. Several methods are used to extract the phase of the modulated waveform, such as the phase-lock loops or more complicated systems as illustrated in Figure 6

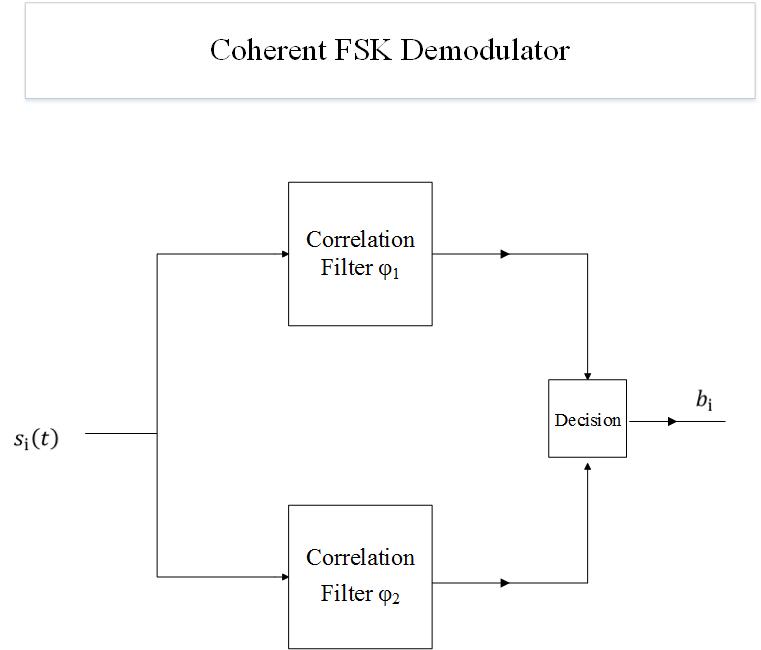


Figure 6. Coherent modulator for BFSK. The data *m(t)* controls the output of the VCO through Eq.

The coherent demodulator uses two parallel branches for matching the Space and Mark unto the two orthonormal basis functions. Finally, using the appropriate threshold, the bits can recovered using Maximum Likelihood. The correlation filters are designed to be orthonormal to each other, and at the same frequency corresponding the Mark and Space.

### Systems A, B, & C (AWGN Channel)

Deep space and satellite communication links are riddled with random errors across a very wide bandwidth (Nguyen, et. al, 2009). In addition to random errors in the satellite link, bursts of noise can corrupt an entire segment of a link resulting in burst errors (Murphy, et. al, 1994). These channel imperfections are common in satellite communications and are modeled very well by the additive white Gaussian noise (AWGN) channel (Viswanathan, 2013). The AWGN channel is a random noise channel that makes a communication link vulnerable to random bit errors and burst errors. In general, it is understood that AWGN provides maximum bit corruption and compared to other channel models, systems that perform the best in AWGN perform the best in real-life situations (Viswanathan, 2013). Hence, this senior design project will rely solely on the AWGN channel (see Section 1.3.6) to represent the propagation medium for our three amateur radio satellite telemetry systems.

### System C (FEC Engine)

Forward error correction (FEC) is a form of robust channel coding. It is used to correct errors that are injected into a digital communication link across a noisy propagation medium. FEC codes fall into two general categories: block codes and convolutional codes. It is important to note that at the time of writing this document, the Xilinx CORE Generator in Project Navigator ISE 14.6 only consists of one block coder/decoder pair and one convolutional coder/decoder pair. The block coding pair consists of a Reed-Solomon coder and decoder. The convolutional coding pair consists of a convolutional encoder and a Viterbi decoder. Hence, the FEC engine will be limited to using these channel code pairs.

In Section 1.3.5, we discussed that the satellite communication link is vulnerable to random errors and burst errors. Block codes are better suited for correcting burst errors while convolutional codes are better suited for correcting random errors (Viswanathan, 2013). A combination of block codes and convolutional codes, namely a two-level coding system, are used in many systems to provide robustness against both kinds of errors (see Figure 7). This two-level coding system consists of a coding chain and a decoding chain. The coding chain resides in the transmitter and consists of a Reed-Solomon encoder, followed by an interleaver, then a convolutional encoder. The decoding chain resides in the receiver and undoes what the coding chain did. Namely, the decoding chain consists of a Viterbi (convolutional) decoder, followed by a de-interleaver, then a Reed-Solomon decoder.



Figure 7. Top-level diagram for the FEC engine (System C) consisting of a block code pair, an interleaving pair, and a convolutional code pair.

### Systems A, B, & C (BERT)

We implement the bit error rate tester (BERT) in software. The BERT consists of an AX.25 packet generation program written by us, a custom AX.25 packet comparison program written by us, and an available virtual serial terminal interface (with data logging capabilities). The BERT provides several performance metrics based off of bit error rate (BER) and packet error rate (PER). Please refer to Section 3 (Approach) for the implementation of this BERT and how it interfaces with the external FPGA board.

**EVERYTHING FOLLOWING THIS SECTION (1.3.7) MUST BE MODERATELY MODIFIED TO REFLECT THE NEW OVERALL OBJECTIVE (EFFECTIVE: 11/06/13). PLEASE BE AWARE OF THIS WHEN READING THE REST OF THIS DOCUMENT.**

## Proposed Solution Concept

In order to provide Temple University’s radio club with a robust and reliable modem, it must be able to be interfaced with a transceiver and the TNC. This requires a single analog to digital converter for received signals and a single digital to analog converter for transmitted signals. Figure 7. Illustrates the how the 1200pbs modem fits into the system level model



Figure 7. System level diagram showing how the 1200bps modem interfaces with the transceiver and TNC.

The Xilinx Spartan-6 LX-9 Microboard was selected for our modem implementation because of its good performance and low cost. It also provides the two Pmod expansion ports needed for interfacing Digilent’s 12-bit AD1 ADC and 12-bit DA2 DAC.

It was determined through simulation that optimum coherent demodulation was achieved from the use of a (squaring or Costas) loop. The result is a modem design that incorporates a bi-phase Manchester encoder for baseband modulation of AX.25 data streams, and a (squaring or Costas) loop for coherent demodulation of BPSK signals.

## Major Design and Implementation Challenges

The biggest design challenge associated with this project is the development of a carrier reconstruction circuit that is capable of mitigating the effects of Doppler shift. The relative motion of satellites in orbit around earth with respect to the ground station can cause the received frequency to appear 20 kHz above or below its nominal downlink frequency. In John A. Maglicane’s 1993 design, he derived a control signal from the carrier recovery circuit that simulated a person tuning the transceivers frequency control button. In our design, Doppler shift correction will be done autonomously through the use of a type II PLL.

The challenge is designing a stable control loop that minimizes time to lock and inter-symbol interference but still has a narrow enough bandwidth to reduce noise and the bit error rate. Since the PLL is an inherently non-linear system, it must be linearized in terms of the phase of the received signal. This problem becomes more challenging if the Costas loop is implemented because the arm filters much be matched perfectly. However, the advantage of an all digital Costas loop is that designing two identical filters is much easier than if it were done with analog components.

## Implications of Project Success

The successful design of a 1200bps modem will enable Temple University Amateur Radio club to communicate with LEO-AMSATs that use FSK for uplink and BPSK for downlink. Although software is available that will perform the modem functions, an FPGA modem demonstrates the potential for high speed processing in re-programmable logic circuitry.

# DESIGN REQUIREMENTS

## Functional Design Constraints

|  |  |
| --- | --- |
| **Name** | **Description** |
| Bit Rate | Provides 1200 b/sec data rate to meet LEO-AMSAT telemetry requirements |
| FEC |  |
| Modulation Type | Supports BPSK and FSK modulation and Demodulation |
| Operating Frequencies | The modulator and demodulator will provide operation between 1200 Hz and 2400 Hz in accordance with the Bell 202 standard |
| Interface |  |
| Signal to Noise (SNR) |  |
| Bit Error Rate |  |

Table 2. Functional design constraints for the GADGET system.

## Non-Functional Design Constraints

|  |  |  |
| --- | --- | --- |
| **Type** | **Name** | **Description** |
| Economic | Cost |  |
| Environmental | Temperature |  |
| Environmental | Power Consumption |  |
| Manufacturability | Dimensions |  |
| Manufacturability | Weight |  |

Table 3. Non-functional design constraints for the GADGET system.

# APPROACH

**Here, will be an introduction and summary of our design approach from high-level Simulink blocks to lower level hardware realizable Xilinx blocks, and then finally delving into hardware implementation. The approach is divided into TWO major sub-sections, *Software Simulation Using Matlab/Simulink* and *Hardware Implementation Using Xilinx ISE Design Suite*. The first subsection WILL be completed by DEC 2. The second sub-section will be completed in SDII.**

## Software Simulation Using Matlab/Simulink

### FSK Modem

### BPSK Modem

### Interleaving FEC

## Hardware Implementation using ISE Design Suite

# EVALUATION

# SUMMARY AND FUTURE WORK

# ACKNOWLEDGEMENTS

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1. Product SPECIFICATION
2. SOME INTERESTING RELEVANT DERIVATION