Design Document

**Forward Error Correction and Interleaving in**

**Amateur Radio Satellite Telemetry**

Submitted To:

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Senior Design Project I and II

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**Executive Summary**

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# Problem

## Overall Objectives

It has been shown that forward error correction dramatically improves bit error rate performance in amateur packet radio satellite telemetry links (Hsiao, et. al, 2000). This senior design project aims to demonstrate how interleaving techniques can further improve the reliability of these telemetry links. Consequently, this senior design project advocates for improved robustness in amateur packet radio communication systems, specifically in those systems dealing with satellite telemetry. Amateur packet radio satellite telemetry is often unidirectional and does not benefit from automatic repeat request (ARQ) like in other bidirectional amateur packet radio communications (Hsiao, et. al, 2000). In other words, if even one bit of an AX.25 telemetry packet is received in error, the entire packet is discarded and cannot be re-transmitted (Karn, 1994). This means that beacon signals from the amateur satellites must be transmitted with enough power to ensure that the embedded telemetry packet is received without error (Milliano, et. al, 2010).

Forward error correction combined with interleaving could greatly improve both network reliability and power-efficiency in amateur packet radio satellite telemetry. The enhanced network reliability could lower overall power consumption in amateur telemetry satellites (Milliano, et. al, 2010), resulting in two benefits: 1) reduced cost of satellite construction, and 2) making amateur telemetry satellites more accessible to amateur satellite operators by reducing the size, cost, and complexity of ground station antennas (Karn, 2011). Hence, the ultimate goal of this senior design project is to demonstrate the improved network reliability and power-efficiency that results from implementing forward error correction and interleaving in amateur radio satellite telemetry satellites and ground stations.

## Historical and Economic Perspective

[TO BE COMPLETED AS OF 11/06/13]

**EVERYTHING FOLLOWING THIS SECTION (1.2) MUST BE MODERATELY MODIFIED TO REFLECT THE NEW OVERALL OBJECTIVE (EFFECTIVE: 11/06/13). PLEASE BE AWARE OF THIS WHEN READING THE REST OF THIS DOCUMENT.**

## Candidate Solutions

The LEO-AMSAT’s that we are interested in communicating with are also known as packet satellites (PACSAT). This is because they use the AX.25 protocol which transmits packets of data. Packets are also known as frames and each frame consists of several fields. These fields include flag, control, and address information in addition to the data to be sent. Since Terminal Node Controllers (TNC) are responsible for AX.25 encoding and already contain a modem within, we originally considered an FPGA implementation of a TNC. However, the complexity and depth of the AX.25 protocol in addition to a modem design wash determined to be too ambitious given the time constraint of two semesters. Instead, we simply chose to design an FPGA modem that would interface with the TNC and transceiver.

### BPSK modulator

The design of any modem requires two fundamental components, a modulator and demodulator. The modulator is responsible for taking baseband data and either source encoding it, or translating it to passband levels necessary for radio transmission. In the history of digital communication, there are many line codes that have been developed. Each of them has their own benefits as far as bandwidth requirements or self-clocking characteristics. Listed below are just a few of the more common line codes typically encountered in a communication systems:

1. Return to Zero (RZ)
2. Non-Return to Zero (NRZ)
3. Non-Return to Zero-Inverted (NRZI)
4. Bi-phase Manchester

Our modem was designed to interface between the TNC and the transceiver. This means our modem will only perform baseband modulation. From the TNC, the modem receives AX.25 data streams and further processes them using a bi-phase Manchester encoder. The benefit of bi-phase Manchester code is that it is self-clocking which makes timing synchronization easier on the receiving end.

### BPSK demodulator

The demodulator is responsible for providing either coherent or non-coherent demodulation. Coherent demodulators require phase synchronization between the received signal and the locally generated oscillator. Conversely, Non-coherent demodulation does not require synchronization and makes no attempt to estimate the phase of the received signal. The advantage of non-coherent modulation is that it does not require additional hardware like phase-locked loops which are used to lock onto the incoming carrier phase. However, the LEO-AMSAT’s we are interested in communicating with use BPSK for downlink and thus requires the design of a coherent demodulator.

The successful extraction of information from a received signal in a coherent demodulator requires both carrier and timing synchronization. Figure 1 illustrates the architecture of a typical coherent demodulator.



Figure 1. Received waveform takes two paths. First path extracts carrier for coherent demodulation and the second path recovers timing information. This architecture is based on the optimum binary receiver

The received signal from the transceiver is first processed by a band pass filter to remove as much noise as possible and then sent to the carrier recovery circuit. Recovering the carrier is done in one of two ways, the squaring loop or the Costas loop. Each method utilizes phase-lock concepts and has its own advantages and disadvantages in terms of complexity and performance.

### Carrier Recovery using Squaring Loop

The squaring loop is a popular choice for coherent demodulation of BPSK waveforms. It’s mathematically easy to analyze and its hardware implementation is not as complex as the Costas loop. As the name implies, the received signal is squared to remove any phase offsets and then processed by a bandpass filter to remove as much noise as possible. After the band pass filter, the signal is fed to a phase-lock loop (PLL) for phase and frequency tracking. Once the output of the voltage controlled oscillator (VCO) is locked in phase and frequency with the received signal, its frequency is divided by two. The resulting carrier is fed back to the mixer where it is mixed with the received waveform and the timing can be recovered. The operation of the squaring is shown in Figure 2.



Figure 2. Squaring loop used for carrier recovery in the coherent demodulator. The Phase-Lock Loop utilizes feedback to track and lock onto in the received waveforms suppressed carrier

### Carrier Recovery using Costas Loop

Another method for carrier recovery was proposed by John P. Costas in his 1957 paper, *Synchronous Communication*. Unlike the squaring loop whose only purpose is suppressed carrier reconstruction, the Costas loop is capable of synchronous data detection in addition to suppressed carrier reconstruction. One of its disadvantages is its mathematical complexity compared to the squaring loop, but in terms of hardware components needed for complete coherent demodulation, they both require approximately the same amount.



Figure 3. Costas loop used for suppressed carrier reconstruction as well as synchronous data detection.

Coherent modulation utilizing the Costas loop would require one band-pass filter, three low-pass filters, three multipliers and a VCO. Likewise, the squaring loop would also require one band-pass filter, three multipliers (including the squarer) and a VCO. Instead of three low-pass filters needed by the Costas, the squaring loop only requires two. Note also that the squaring loop requires a flip-flop for frequency division, but with today’s FPGA’s, a single flip-flop is negligible. The decision for implementing the squaring loop versus the Costas loop will ultimately be decided by their tracking and locking performance in the presence of noise and Doppler shifts (See section 1.5, Major Design and Implementation Challenges).

### Timing Recovery

### BFSK Modulation

The BFSK modem abides by the Bell 202 standard which uses frequencies of 1200 Hz for Mark (*b0*) and 2200 Hz for Space (*b1*). Following this protocol, the phase of the signal can be implemented either coherently or non-coherently. A coherent modulation (continuous phase modulation) implies that the phases of the two signals are always equal, which inherently prevents discontinuous jumps between a Mark and Space. Conversely, non-coherent FSK modulates the two signal waveforms without any effort to match the two signals’ phase, hence the modulated signal may experience discontinuous jumps in phase.

Coherent FSK modulators tend to consist of several complicated components, are not commonly used to avoid unnecessary loss of power although they yield a better BER performance (Rao, 1990). Non-coherent FSK modulation is simpler to implement and is commonly used in several modulation. However, with the technological development, coherent modulation can surely be implemented with as much efficiency as the non-coherent modulation.

**Non-coherent modulation**

As previously mentioned, coherent modulation requires continuous phase of the modulated signal, which can involve complicated hardware or algorithms. As a result, it is common to ignore the phase of the signals and directly modulate the two signals. This implies that the phase modulated signal will be subject of random variations. The non-coherent modulator can be implemented using the two sinusoidal wave generators (sine functions) and a multiplexer controlled by the input data *m(t)*. Switching between the frequencies will generate a BFSK waveform with a bit period equal to the periodicity of the switches.



Figure 4. BFSK modulator used in non-coherent modulators. The data *m(t)* controls the output of the multiplexer at data’s baud rate.

**VCO Coherent modulation**

Non-coherent waveforms originate from the fact that two signal sources are used to modulate the data, therefore the phase resulting from the modulator varies with the phases of the two tones. Therefore, we expect that continuous phase can be obtained when using a single sinusoidal generator to modulate with two different frequencies. Voltage Control Oscillators

### BFSK Demodulation

In the case of the coherent modulator, implementing a continuous phase BFSK waveform may involve complicated elements to track the phase; however, a continuous phase waveform or (glitch free) will enhance error performance compared to the non-coherent modulator. It is very common to implement the coherent modulator using a Voltage Controlled Oscillator (VCO) to output the sinusoidal corresponding to the Mark and Space. Since the VCO is dictated by Eq. only one sinusoidal wave generator is necessary to create two signals.

The Bell 202 Protocol is quite inefficient due to the frequency deviation and the ratio between the data rate and carrier frequency. The Bell 202 modem uses frequencies with a small frequency deviation from the carrier frequency. with very smal the Bell 202 modem The frequencies selected to represented two symbols result in a signal space that is difficult to optimize since the frequencies are not orthogonal. The minimum frequency separation is denoted in equations (1) and (2) below (Nguyen, 2009).



Figure 5. Coherent modulator for BFSK. The data *m(t)* controls the output of the VCO through Eq.

Non-Coherent Demodulation

Similar to the modulator, the demodulator can be classed into a coherent modulator and a non-coherent demodulator. In the coherent demodulator, the phases of the modulated signal is either known or is extracted prior to demodulation. Several methods are used to extract the phase of the modulated waveform, such as the phase-lock loops or more complicated systems as illustrated in Figure 6

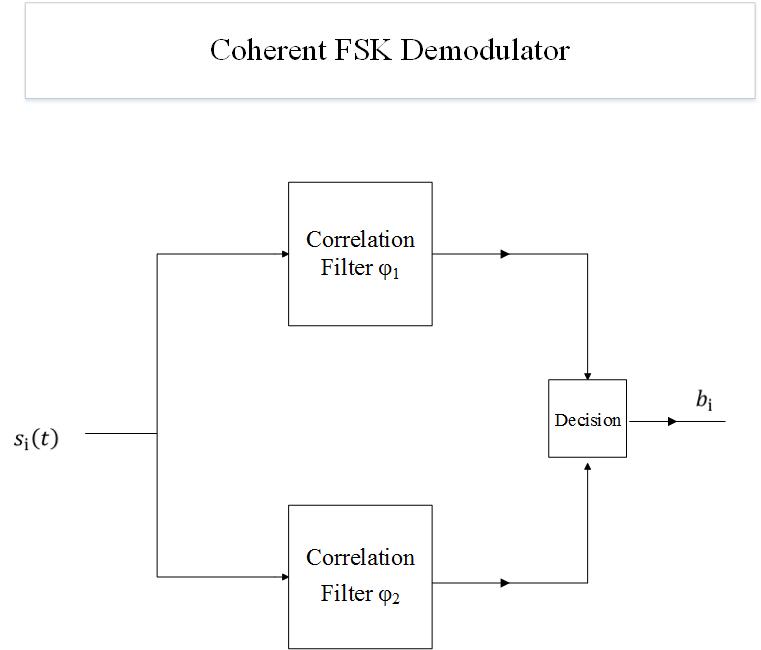


Figure 6. Coherent modulator for BFSK. The data *m(t)* controls the output of the VCO through Eq.

The coherent demodulator uses two parallel branches for matching the Space and Mark unto the two orthonormal basis functions. Finally, using the appropriate threshold, the bits can recovered using Maximum Likelihood. The correlation filters are designed to be orthonormal to each other, and at the same frequency corresponding the Mark and Space.

## Proposed Solution Concept

In order to provide Temple University’s radio club with a robust and reliable modem, it must be able to be interfaced with a transceiver and the TNC. This requires a single analog to digital converter for received signals and a single digital to analog converter for transmitted signals. Figure 7. Illustrates the how the 1200pbs modem fits into the system level model



Figure 7. System level diagram showing how the 1200bps modem interfaces with the transceiver and TNC.

The Xilinx Spartan-6 LX-9 Microboard was selected for our modem implementation because of its good performance and low cost. It also provides the two Pmod expansion ports needed for interfacing Digilent’s 12-bit AD1 ADC and 12-bit DA2 DAC.

It was determined through simulation that optimum coherent demodulation was achieved from the use of a (squaring or Costas) loop. The result is a modem design that incorporates a bi-phase Manchester encoder for baseband modulation of AX.25 data streams, and a (squaring or Costas) loop for coherent demodulation of BPSK signals.

## Major Design and Implementation Challenges

The biggest design challenge associated with this project is the development of a carrier reconstruction circuit that is capable of mitigating the effects of Doppler shift. The relative motion of satellites in orbit around earth with respect to the ground station can cause the received frequency to appear 20 kHz above or below its nominal downlink frequency. In John A. Maglicane’s 1993 design, he derived a control signal from the carrier recovery circuit that simulated a person tuning the transceivers frequency control button. In our design, Doppler shift correction will be done autonomously through the use of a type II PLL.

The challenge is designing a stable control loop that minimizes time to lock and inter-symbol interference but still has a narrow enough bandwidth to reduce noise and the bit error rate. Since the PLL is an inherently non-linear system, it must be linearized in terms of the phase of the received signal. This problem becomes more challenging if the Costas loop is implemented because the arm filters much be matched perfectly. However, the advantage of an all digital Costas loop is that designing two identical filters is much easier than if it were done with analog components.

## Implications of Project Success

The successful design of a 1200bps modem will enable Temple University Amateur Radio club to communicate with LEO-AMSATs that use FSK for uplink and BPSK for downlink. Although software is available that will perform the modem functions, an FPGA modem demonstrates the potential for high speed processing in re-programmable logic circuitry.

# DESIGN REQUIREMENTS

## Functional Design Constraints

## Non-Functional Design Constraints

# APPROACH

# EVALUATION

# SUMMARY AND FUTURE WORK

# ACKNOWLEDGEMENTS

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1. Product SPECIFICATION
2. SOME INTERESTING RELEVANT DERIVATION